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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,524	08/09/2000	Hiroyuki Takahashi	P19483	5635

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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	PAPER NUMBER
2189	4

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/635,524	TAKAHASHI, HIROYUKI	
	Examiner	Art Unit	
	Christopher E. Lee	2189	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 August 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to because there are not labels for the flow directions after the decision boxes 2802, 2805, and 2807 in Fig. 28. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 8 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for scrapping return-address, temporarily stored in the stack memory area of the RAM, without being restored into the program counter, and jumping to the instruction for calling the next subroutine (See Application, page 70, lines 1-15, and Fig. 31, steps J3 and J4), does not reasonably provide enablement for setting the comparison address data (i.e., address data of the defective part in the ROM) as a return-address data in the program counter when the interruption-processing is completed (See claim 8). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. Furthermore, the claim 8 recites the limitation "an address-coincidence-disabling system that disables the coincidence between said comparison address data and said return-address set in said program counter by said return-

address-setting system", which causes that the claimed invention cannot achieve the objective of the applicant's invention, such that the objection of the applicant's invention is to provide a microcomputer with a program-revision ability, wherein a revision can be made in an optional location of programs stored in a ROM thereof (See Application, page 4, line 23 through page 5, line 1), because said controller/calculator (i.e., CPU) would fetch and execute the defective part of ROM after completion of the revision execution, i.e., the program counter has been set said comparison address data (i.e., address data of the defective part in ROM) as the return address of the interrupt-processing when the interruption-processing has been completed (See claim 8).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimada et al. [US 6,237,120 B1; hereinafter Shimada].

Referring to claim 1, Shimada discloses a microcomputer (i.e., electronics apparatus in Fig. 2) including a read-only memory (i.e., ROM 15 of Fig. 2) that stores programs (i.e., firmware; See col. 3, lines 55-57 and 61-63), a controller/calculator (i.e., CPU 14 of Fig. 2) that successively accesses to addresses of said programs (i.e., firmware) stored in said read-only memory (i.e., ROM) to retrieve and decode an instruction from each of said accessed addresses, thereby executing a processing based on said decoded instruction (See col. 1, lines 28-32), and a program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2) in which an address to be accessed by said controller/calculator is successively renewed and indicated (See col. 3, lines 39-40 and col. 6, lines 41-45), said

microcomputer comprising: at least one comparison-address-storage device (i.e., correcting address storing unit 3 of Fig. 1, which corresponds 16-bit interruption generating address register 21 of Fig. 2) that stores a comparison address data (i.e., correcting address) corresponding to an optional address of said programs stored in said read-only memory (i.e., address of defective portion of the firmware stored in ROM; See col. 3, lines 51-59), at which an interruption-processing should be executed to virtually revise said programs stored in said read-only memory (See col. 4, lines 23-34); a random-access memory (i.e., RAM 26 of Fig. 2) that stores a revisional program (i.e., correcting contents in RAM) in which said interruption-processing is programmed (See col. 4, lines 7-9); at least one vector-address-storage device (i.e., interruption vector register 23b of Fig. 2) that stores a vector address (i.e., interruption vector) data corresponding to a head address (i.e., leading address of said correcting content stored in RAM) of said revisional program stored in said random-access memory (See col. 4, lines 35-38); and an address comparator (i.e., comparator 22 of Fig. 2) that compares said comparison address data (i.e., correcting address) with an address successively renewed in said program counter (i.e., execution address on Address Bus 16; See col. 4, lines 12-15), wherein said controller/calculator (i.e., CPU) makes an access to said head address of said revisional program (i.e., leading address of patch for correcting contents in RAM), stored in said random-access memory, corresponding to said vector address data stored in said vector-address-storage device (See col. 4, lines 31-34), when it is determined by said address comparator that there is a coincidence between said comparison address data and said renewed address of said program counter (See col. 4, lines 12-17), resulting in an execution of said interruption-processing in accordance with said revisional program (See col. 4, lines 31-52).

Referring to claim 2, Shimada teaches a discrimination system (i.e., control flag latch 23a of Fig. 2) that discriminates whether said coincidence between said comparison address data and said renewed address of said program counter is proper (See col. 4, lines 23-27; i.e., the control flag latch (discrimination system) indicates (discriminates) whether a defective portion exists within the ROM (i.e.,

said coincidence is proper)); and an address-coincidence-disabling system (i.e., switch 24 of Fig. 2) that disables said coincidence between said comparison address data and said renewed address of said program counter (i.e., the coincidence signal is disabled by the switch open; See col. 4, lines 27-34).

Referring to claim 3, Shimada teaches a rewritable and non-volatile memory (i.e., EEPROM 27 of Fig. 2) that stores said revisional program, said comparison address data and said vector address data (See col. 4, lines 56-57); a reading/writing system (i.e., communication circuit 29 of Fig. 2) that reads said revisional program, said comparison address data and said vector address data from said rewritable and non-volatile memory, and then writes these data in said random-access memory, said comparison-address-storage device and said vector-address storage device, respectively (See col. 3, line 66 through col. 4, line 11), whenever said microcomputer is powered ON (See col. 6, lines 1-7).

Referring to claim.4, Shimada teaches said address comparator (i.e., comparator 22 of Fig. 2) is connected to said program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2) to thereby retrieve said renewed address therefrom (i.e., retrieving execution address (renewed address) on Address Bus 16, which is connected said program counter; See col. 4, lines 12-15).

Referring to claim 5, Shimada teaches said address comparator is connected to an address bus (i.e., Address Bus 16 of Fig. 2) extending to said program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2) to thereby retrieve said renewed address therefrom (i.e., retrieving execution address (renewed address) on Address Bus 16, which is connected said program counter; See col. 4, lines 12-15).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada [US 6,237,120 B1].

Referring to claims 6 and 7, Shimada teaches a vector-address data setting system (i.e., interruption control circuit 25 of Fig. 2) that reads said vector address data from said vector-address-storage device, and is then set in said program counter (See col. 4, lines 30-34; i.e., the coincidence signal input to the interruption control circuit as an interrupt request signal and the control by the CPU is moved to the address shown by an interrupt vector register by the interruption processing in the interrupt control unit implies that said vector-address data setting system reads said vector address data from said vector-address-storage device, and is then set in said program counter).

Shimada does not expressly show a vector-address-temporary-storage device that receives said vector address data from said vector-address-storage device, when it is determined by said address comparator that there is said coincidence between said comparison address data and said renewed address of said program counter.

However, Shimada teaches said vector-address-storage device (i.e., interruption vector register 23b with 16-bits width in Fig. 2) coupled to a data bus (i.e., data bus 13 with 8-bits width in Fig. 2) is loaded into said program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2) coupled to an address bus (i.e., Address Bus 16 with 16-bits width in Fig. 2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have included said vector-address-temporary-storage device in said controller/calculator (i.e., CPU 14 of Fig. 2), which receives said vector-address data from said vector-address-storage device, when it is determined by said address comparator that there is said coincidence between said comparison address data and said renewed address of said program counter (i.e., when the interrupt occurs) since said data bus (8-bits width) cannot support a direct transfer (viz., single transferring transaction) of said vector address data (16-bits width) from said vector-address-storage device (16-bits width) to said program counter (16-

bits width) without said vector-address-temporary-storage device, which could be temporarily holding (viz., buffering) and assembling two 8-bits width said vector-address data into a single 16-bits width said vector-address data for said 16-bits width said program counter and its coupled address bus.

Therefore, Shimada teaches said vector-address data setting system (i.e., interruption control circuit 25 of Fig. 2) that reads said vector address data from said vector-address-temporary-storage device, and is then set in said program counter (See col. 4, lines 30-34; i.e., the coincidence signal input to the interruption control circuit as an interrupt request signal and the control by the CPU is moved to the address shown by an interrupt vector register by the interruption processing in the interrupt control unit implies that said vector-address data setting system reads said vector address data from said vector-address-temporary-storage device, and is then set in said program counter).

However, the recitation in the claims 6 and 7 "whereby said access to said head address of said revisional program by said controller/calculator is made, resulting in said execution of said interruption-processing in accordance with said revisional program" has not been given patentable weight, respectively, because it has been held that the functional "whereby" statement does not define any structure and accordingly cannot serve to distinguish. *In re Mason, 114 USPQ 127, 44 CCPA 937 (1957).*

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure with regarding to a firmware patching technology.

Esfahani et al. [US 6,434,695 B1] disclose computer operating system using compressed ROM image in RAM.

Neal et al. [US 6,154,834 A] disclose detachable processor module containing external microcode expansion memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

CEL/
April 5, 2003

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